UNITED STATES PATENT APPLICATION

OF

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FOR

LIQUID CRYSTAL DISPLAY AND FABRICATING METHOD

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[0001] This application claims the benefit of Korean Patent Application No. 2000-85273, filed on December 29, 2000, the entirety of which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] This invention relates to a liquid crystal display, and more particularly to a liquid crystal display and a fabricating method thereof that are capable of realizing a high aperture ratio as well as implementing a high-density storage capacitor.

Description of the Related Art

[0003] Generally, a liquid crystal display (LCD) controls the light transmissivity of a liquid crystal cell in response to a video signal to display a picture. An active matrix LCD having a switching device for each liquid crystal cell is suitable for displaying a moving picture. The active matrix LCD mainly uses a thin film transistor (TFT) as the switching device. Since such an active matrix LCD can be made into a smaller device in size than the existent Brown tube or Cathrode Ray Tube (CRT), it has been widely used for a personal computer or a notebook computer as well as office automation equipment such as a copy machine, and portable equipment such as a cellular phone and a pager.

[0004] Referring to FIG. 1 and FIG. 2, the conventional LCD includes a gate line 2 and a data line 4 formed on a substrate 1 to cross each other, a TFT arranged at an intersection between a data line 4 and a gate line 2, and a storage capacitor overlapping with the gate line 2.

[0005] The gate line 2 and the data line 4 are electrically isolated from each other by a gate insulating film 9. Each pixel is driven by the TFT and electrically

connected to the gate line 2 and the data line 4.

[0006] The TFT includes a gate electrode 54, a source electrode 51, a drain electrode 52, an active layer 5 and an ohmic contact layer 10. The gate electrode 54 is connected to the gate line 2. The gate insulating film 9 is entirely deposited onto the substrate 1 to cover the gate electrode 54 and the gate line 2. The active layer 5 and the ohmic contact layer 10 are formed on the gate insulating film 9 to overlap with the gate electrode 54. The source electrode 51 is connected to the data line 4 while the drain electrode 52 is opposed to the source electrode 51 having a desired channel size therebetween.

[0007] A protective layer 53 is entirely deposited onto the gate insulating film 9 to cover the gate line 2, the data line 4 and the TFT. A pixel electrode 55a is connected to the drain electrode 52 via a first contact hole 8, and is provided on the protective layer 53.

[0008] The storage capacitor is charged by a voltage on the previous gate line 2 upon scanning of the previous scanning line to apply the charged voltage to the pixel electrode 55a upon scanning of the following scanning line. The storage capacitor includes the gate line 2 and a storage electrode 6 opposed to each other having the gate insulating film 9 therebetween. The storage electrode 6 is connected to a transparent electrode pattern 55b via a second contact hole 18 defined on the protective layer 53. The transparent electrode pattern 55b is patterned simultaneously with the pixel electrode 55a.

[0009] FIG. 3A to FIG. 3E are sectional views for explaining a method of fabricating the LCD device shown in FIG. 2.

[0010] Referring first to FIG. 3A, the gate electrode 54 and the gate line 2 are provided on the substrate 1. The gate electrode 54 and the gate line 2 are formed by entirely depositing a metal such as aluminum (Al) or copper (Cu), etc. onto the substrate 1 and then patterning it.

[0011] Referring to FIG. 3B, the active layer 5 and the ohmic contact layer 10 are provided on the gate insulating film 9.

[0012] The gate insulating film 9 is formed by depositing an insulating material such as silicon nitride (SiN_x) or silicon oxide (SiO_x) and then patterning it. The active layer 5 is formed from amorphous silicon that is not doped with an impurity. In contrast, the ohmic contact layer 10 is formed from amorphous silicon doped with an n-type or p-type impurity at a high concentration.

[0013] The active layer 5 and the ohmic contact layer 10 are formed by depositing first and second semiconductor material layers after forming the gate insulating film 9 on the substrate 1 to cover the gate electrode 54 and then patterning them.

[0014] Referring to FIG. 3C, the data line 4 (not shown), the storage electrode 6, the source electrode 51 and drain electrode 52 are provided on the gate insulating film 9. The source electrode 51 and drain electrode 52 are formed by entirely depositing a metal layer such as chromium (Cr) or molybdenum (Mo) using a chemical vapor deposition (CVD) technique or a sputtering technique and then patterning it. After the source electrode 51 and drain electrode 52 were patterned, the ohmic contact layer 10 is formed at an area corresponding to the gate electrode 54 and is also patterned to expose the active layer 5. A portion of the active layer 5 exposed by the source electrode 51 and drain electrode 52 serves as a channel. The data line 4 (not shown), the storage electrode 6, the source electrode 51 and drain electrode 52 are made from a metal such as chromium (Cr) or molybdenum (Mo).

[0015] Referring to FIG. 3D, the protective layer 53 and the first contact hole 8 and second contact hole 18 are provided on the gate insulating film 9.

[0016] The protective layer 53 and the first contact hole 8 and second contact hole 18 are formed by depositing an insulating material on the gate insulating film 9 to cover the source electrode 51 and drain electrode 52 and then patterning it. The

protective layer 53 is made from an inorganic insulating material such as silicon nitride (SiN_x) or silicon oxide (SiO_x), or an organic insulating material having a small dielectric constant such as an acrylic organic compound, Teflon, benzocyclobutene (BCB), Cytop or perfluorocyclobutane (PFCB).

[0017] The protective layer 53 is provided with the first contact hole 8 and second contact hole 18. The first contact hole 8 is defined to pass through the protective layer 53, to thereby expose a portion of the surface of the drain electrode 52. Similarly, the second contact hole 18 is defined to pass through the protective layer 53, to thereby expose a portion of the surface of the storage electrode 6.

[0018] Referring to FIG. 3E, the pixel electrode 55a is provided on the protective layer 53. The pixel electrode 55a is formed by depositing a transparent conductive material such as indium-tin-oxide (ITO), indium-zinc-oxide (IZO) or indium-tin-zinc-oxide (ITZO) on the protective layer 53 and then patterning it. The pixel electrode 55a is electrically connected, via the first contact hole 8, to the drain electrode 52, and is electrically connected, via the second contact hole 18, to the storage electrode 6.

[0019] In such an LCD, the storage electrode 6 should have a sufficiently large capacitance value so that it can reduce variation in a data voltage charged in the pixel electrode 55a. Although the storage electrode 6 is extended into a pixel area to increase its capacitance value, the pixel area is narrowed by the extension of the storage electrode 6 into the pixel area, thus reducing aperture ratio. Moreover, since black matrices provided on the upper glass substrate to protect light leakage between the pixels overlap with the pixel area by approximately 5μm at the left/right end and the upper/lower end of the pixel electrode 55a, the pixel area is reduced by the overlap and, hence, aperture ratio is reduced.

[0020] FIG. 4 represents an equivalent circuit of a pixel cell in the LCD.

[0021] In FIG. 4, a value of a storage capacitor Cst for keeping a voltage drop

Vdrop within 80mV (i.e., 1 gray voltage of 64 gray levels) can be given by the following equations:

$$V_{lc}(t)= V_{lc}(0)[Exp(-T_f/R_{off}C_t)] \text{ (If } V_{drop}= V_{lc}(0)- V_p(t)) \quad \ldots (1)$$

wherein Vlc represents a liquid crystal driving voltage; Tf is one frame interval; Roff is an internal resistance; Vp is a pixel voltage; Vdrop is a voltage drop; and Ct is total capacitor value (i.e., liquid crystal capacitance, Clc + storage capacitor value Cst).

$$V_{drop}= V_{lc(0)}[1-Exp(-T_f/R_{off}C_t)] \quad \ldots (2)$$

wherein Vdrop represents a voltage drop; Tf is one frame interval; Vlc is a liquid crystal driving voltage; and Ct is total capacitor value.

$$C_t>(T_f/R_{off})/L_n[V_i/(V_i-V_{drop})] \quad \ldots (3)$$

wherein Ln represents an inductance; and Vi is an initial voltage.

[0022] In equation (3), Ct = Clc + Cst; Tf = 16.7ms (1 frame interval); Vlc = 5V; Vdrop = 80mV; and Roff = Vi/Ioff = 5V/4pA = 1.25E + 12Ω.

[0023] Table 1 describes an area and an occupied ratio of the storage capacitor according to a resolution when a thickness of the gate insulating film 9 formed between the storage electrode 6 and the gate line 3 in a high-resolution LCD shown in FIG. 1 is 4000Å.

Table 1

	Sub-Pixel size	Clc	Requested minimal Cst	Storage size	Occupied ratio
300PPI	2.39E-09	3.4E-14	8.14E-13	5.49E-09	230.0%
250PPI	3.46E-09	5.5E-14	7.93E-13	5.35E-09	154.8%
200PPI	5.29E-09	9.3E-14	7.56E-13	5.10E-09	96.3%
150PPI	9.53E-09	1.8E-13	6.64E-13	4.48E-09	47.0%
100PPI	2.15E-09	4.5E-13	3.95E-13	2.67E-09	12.4%

[0024] It can be seen from Table 1 that, as a resolution increases, a ratio of an area occupied by the storage capacitor within a unit pixel increases. Also, the aperture ratio of the LCD is greatly reduced.

[0025] Table 2 compares a storage capacitor value and an aperture ratio of a high-resolution LCD with those of a ferroelectric liquid crystal display (FLCD) when a thickness of the gate insulating film 9 formed between the storage electrode 6 and the gate line 3 is 4000Å.

Table 2

	200PPI	FLCD MODEL 1	FLCD MODEL 2
Sub-Pixel	5292	25947	25947
Storage	599	2784.5	7113.7
Aperture area	2414	15373.5	11044.3

Aperture ratio	45.60%	59.2%	42.6%

[0026] As can be seen from Table 2, although a storage capacitor value of a ferroelectric liquid crystal display (FLCD) is three times larger than that of a conventional liquid crystal display panel, an aperture ratio of a FLCD is approximately 50% in comparison with that of a conventional liquid crystal display panel.

SUMMARY OF THE INVENTION

[0027] Accordingly, the present invention is directed to a liquid crystal display and fabricating method that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0028] An advantage of the present invention is to provide a liquid crystal display and a fabricating method thereof that are capable of realizing a high aperture ratio as well as implementing a high-density storage capacitor.

[0029] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0030] To achieve these and other advantages of the invention, a liquid crystal display according to one aspect of the present invention includes a data line supplied with a data signal; a gate line supplied with a scanning signal; a pixel electrode for driving a liquid crystal cell; a thin film transistor for applying the data signal to the pixel electrode in response to the scanning signal including a gate insulating film covering the gate line; and a storage electrode formed at the interior of the gate insulating film wherein the storage electrode overlaps with the gate line.

[0031] In the liquid crystal display, a distance between the gate line and the storage electrode is about 500 to 2500Å.

[0032] The liquid crystal display further includes a protective layer formed on the gate insulating film wherein the protective layer covers the data line, the gate line and the thin film transistor.

[0033] In the liquid crystal display, the pixel electrode is connected to the storage electrode via a contact hole passing through the gate insulating film and the protective layer.

[0034] A method of fabricating a liquid crystal display according to another aspect of the present invention includes forming a gate line and a gate electrode of a thin film transistor on a substrate; depositing a first gate insulating film on the substrate to cover the gate electrode and the gate line; forming a storage electrode on the first gate insulating film to overlap with the gate line; depositing a second gate insulating film on the first gate insulating film to cover the storage electrode; forming an active layer and an ohmic contact layer on the gate insulating film; forming a source electrode and a drain electrode of the thin film transistor opposed to each other and having a desired channel therebetween on the ohmic contact layer; forming a protective layer on the gate insulating film to cover the source electrode and the drain electrode; defining a first contact hole for exposing the drain electrode on the protective layer; defining a second contact hole for exposing the storage electrode on the protective layer and the second gate insulating film; and forming a pixel electrode connected to the drain electrode via the first contact hole and connected to the storage electrode on the protective layer via the second contact hole.

[0035] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0036] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0037] In the drawings:

[0038] FIG. 1 is a plan view showing a structure of a conventional high-resolution liquid crystal display;

[0039] FIG. 2 is a sectional view of the liquid crystal display taken along the I-I' line in FIG. 1;

[0040] FIG. 3A to FIG. 3E are views for explaining a method of fabricating the liquid crystal display shown in FIG. 2;

[0041] FIG. 4 is an equivalent circuit diagram for explaining a design of a storage capacitor of a liquid crystal cell in the liquid crystal display;

[0042] FIG. 5 is a plan view showing a structure of a high-resolution liquid crystal display according to an embodiment of the present invention;

[0043] FIG. 6 is a sectional view of the liquid crystal display taken along the II-II' line in FIG. 5; and

[0044] FIG. 7A to FIG. 7F are views for explaining a method of fabricating the liquid crystal display shown in FIG. 6.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0045] Reference will now be made in detail to an embodiment of the present invention, example of which is illustrated in the accompanying drawings.

[0046] FIG. 5 and FIG. 6 are a plan view and a sectional view showing a structure of a high-resolution liquid crystal display (LCD) according to an embodiment of the present invention.

[0047] Referring to FIG. 5 and FIG. 6, the LCD includes a gate line 13 and a data line 14 formed on a substrate 11 to cross each other, a TFT arranged at an intersection between a data line 14 and a gate line 13, and a storage capacitor overlapping with the gate line 13.

[0048] The gate line 13 and the data line 14 are electrically isolated from each other by a gate insulating film 39. Each pixel is driven by the TFT electrically connected to the gate line 13 and the data line 14.

[0049] The TFT includes a gate electrode 64, source electrode 61 and drain electrode 62, an active layer 15, and an ohmic contact layer 20. The gate electrode 64 is connected to the gate line 13. The gate insulating film 39 is entirely deposited onto the substrate 11 to cover the gate electrode 64 and the gate line 13. The active layer 15 and the ohmic contact layer 20 are formed on the gate insulating film 39 to overlap with the gate electrode 64. The source electrode 61 is connected to the data line 14 while the drain electrode 62 is opposed to the source electrode 61, having a desired channel size therebetween.

[0050] A protective layer 63 is entirely deposited onto the gate insulating film 39 to cover the gate line 13, the data line 14 and the TFT. A pixel electrode 65a is connected to the drain electrode 62 via a first contact hole 8, and is provided on the protective layer 63.

[0051] The storage capacitor is charged by a voltage on the previous gate line 13 upon scanning of the previous scanning line to apply the charged voltage to the pixel electrode 65a upon scanning of the following scanning line. The storage capacitor includes the gate line 13 and a storage electrode 16 opposed to each other having the gate insulating film 39 therebetween. The storage electrode 16 is patterned simultaneously with the source electrode 61 and the drain electrode 62. The storage electrode 16 is connected to a transparent electrode pattern 65b via a second contact hole 38 defined on the protective layer 63. The transparent electrode pattern 65b is

patterned simultaneously with the pixel electrode 65a.

[0052] FIG. 7A to FIG. 7F are sectional views for explaining a method of fabricating the LCD shown in FIG. 6.

[0053] Referring first to FIG. 7A, the gate electrode 64 and the gate line 13 are provided on the substrate 11. The gate electrode 64 and the gate line 13 are formed by entirely depositing a metal such as aluminum (Al) or copper (Cu) using a deposition technique such as sputtering and then patterning it.

[0054] Referring to FIG. 7B, the storage electrode 16 and a second gate insulating film 29 are formed on a first gate insulating film 19.

[0055] The first gate insulating film 19 is formed by depositing an insulating material on the substrate 11 to a thickness of about 500 to 2500Å using a process such as plasma enhanced chemical vapor deposition (PECVD) to cover the gate electrode 64 and the gate line 13. The storage electrode 16 is formed in correspondence with the gate line 13 by depositing a metal layer on the first gate insulating film 19 and then patterning it. The second gate insulating film 29 is formed by entirely depositing an insulating material on the first gate insulating film 19 to the same thickness to cover the storage electrode 16.

[0056] The gate insulating film 39 at the TFT area is the total of the thicknesses of the first gate insulating film 19 and the second gate insulating film 29. The total thickness of the gate insulating film 39 is similar to the thickness of the gate insulating film in the conventional art. Accordingly, the gate insulating film 39 between the gate line 13 and the storage electrode 16 is formed at a thickness about half that of the conventional art structure to increase capacitance.

[0057] The first insulating film 19 and second insulating film 29 are formed from an insulating material such as silicon nitride (SiN_x) or silicon oxide (SiO_x). The storage electrode 16 is formed by entirely depositing a metal layer such as chromium (Cr) or molybdenum (Mo) using a CVD technique or a sputtering technique and then

patterning it.

[0058] Referring to FIG. 7C, the active layer 15 and the ohmic contact layer 20 are provided on the gate insulating film 39.

[0059] The active layer 15 and the ohmic contact layer 20 are formed by depositing first and second semiconductor material layers after forming the gate insulating film 39 on the substrate 11 to cover the gate electrode 64 and then patterning them.

[0060] The active layer 15 is formed from the first semiconductor material layer of amorphous silicon that is not doped with an impurity. In contrast, the ohmic contact layer 20 is formed from the second semiconductor material layer of amorphous silicon doped with an n-type or p-type impurity at a high concentration.

[0061] Referring to FIG. 7D, the data line 14 and the source electrode 61 and drain electrode 62 are provided on the gate insulating film 39.

[0062] The source electrode 61 and drain electrode 62 are formed by entirely depositing a metal layer such as chromium (Cr) or molybdenum (Mo) using a chemical vapor deposition (CVD) technique or a sputtering technique and then patterning it. After the source electrode 61 and drain electrode 62 are patterned, the ohmic contact layer 20 is formed at an area corresponding to the gate electrode 64 and also is patterned to expose the active layer 15. A portion of the active layer 15 exposed by the source electrode 61 and drain electrode 62 serves as a channel. The data line 14 and the source electrode 61 and drain electrode 62 are made from a material such as chromium (Cr) or molybdenum (Mo).

[0063] Referring to FIG. 7E, the protective layer 63 and the first contact hole 28 and second contact hole 38 are provided on the gate insulating layer 39.

[0064] The protective layer 63 and the first contact hole 28 and second contact hole 38 are formed by depositing an insulating material on the gate insulating layer 39 to cover the source electrode 61 and drain electrode 62 and then patterning it. The

second contact hole 38 is formed to the same thickness as the first contact hole 28 by patterning the second gate insulating film 29 using the protective layer 63 as a mask to expose the storage electrode 16. The protective layer 63 is made from an inorganic insulating material such as silicon nitride (SiN_x) or silicon oxide (SiO_x), or an organic insulating material having a small dielectric constant such as an acrylic organic compound, Teflon, benzocyclobutene (BCB), Cytop or perfluorocyclobutane (PFCB).

[0065] Referring to FIG. 7F, the pixel electrode 65a and the transparent electrode pattern 65b are provided on the protective layer 63. The pixel electrode and the transparent electrode pattern are formed by depositing a transparent conductive material such as indium-tin-oxide (ITO), indium-zinc-oxide (IZO) or indium-tin-zinc-oxide (ITZO) on the protective layer 63 and then patterning it. The pixel electrode 65a is electrically connected to the drain electrode 62 via the first contact hole 28, and the transparent electrode pattern 65b is electrically connected to the storage electrode 16 via the second contact hole 38.

[0066] In FIG. 7A to FIG. 7F, a distance between the gate line 13 and the storage electrode 16, that is, a thickness of the first gate insulating film 9 is less than the thickness of gate insulating film in the conventional art, reduced to increase a storage capacitor value. Interference between the storage electrode 16 and the pixel area is not required owing to such an increase in a storage capacitor value, so that it becomes possible to improve an aperture ratio. The improvement in aperture ratio according to the present invention can be seen from the following tables.

[0067] Table 3 indicates an aperture ratio of a liquid crystal display according to a thickness of the gate insulating film 39 in the case of a liquid crystal display having a resolution of 200 PPI; and Table 4 and Table 5 indicate aperture ratios of a liquid crystal display according to a thickness of the gate insulating film 39 formed between the gate line 13 and the storage electrode 39 in the case of the first and second models of the ferroelectric (FLC) display.

Table 3

Thickness of gate insulating film between the gate line and the storage electrode (Å)	Storage size (μm^2)	Aperture area (μm^2)	Aperture ratio (%)
4000	599	2414	45.6%
3500	524	2489	47.0%
3000	449	2564	48.4%
2500	374	2639	49.9%
2000	300	2714	51.3%
1500	225	2788	52.7%
1000	150	2863	54.1%
500	75	2938	55.5%

Table 4

Thickness of gate insulating film between the gate line and the storage electrode (Å)	Storage size (μm^2)	Aperture area (μm^2)	Aperture ratio (%)
4000	2784.5	15374	59.2%
3500	2436	15722	60.6%
3000	2088	16070	61.9%

2500	1740	16418	63.3%
2000	1392	16766	64.6%
1500	1044	17114	66.0%
1000	696	17462	67.3%
500	348	17810	68.6%

Table 5

Thickness of gate insulating film between the gate line and the storage electrode (Å)	Storage size (μm^2)	Aperture area (μm^2)	Aperture ratio (%)
4000	7113.7	11044	42.6%
3500	6224	11934	46.0%
3000	5335	12823	49.4%
2500	4446	13712	52.8%
2000	3557	14601	56.3%
1500	2668	15490	59.7%
1000	1778	16380	63.1%
500	889	17269	66.6%

[0068] It can be seen from Table 3 to Table 5 that if a thickness of the gate insulating film 39 formed between the gate line 13 and the storage electrode 16 is reduced to increase a storage capacitor value (Cst) and to decrease a storage area, then

an aperture ratio is improved.

[0069] For instance, in the case of the second model of the FLC display, if a thickness of the insulating film is reduced from 4000Å into 2000Å, then an improvement in an aperture ratio of more than 10% can be obtained.

[0070] As described above, according to the present invention, the storage electrode is formed within the gate insulating film to reduce a thickness between the conductive materials, thereby increasing a capacitance value. Accordingly, the storage capacitor area is set to a small size to thereby improve an aperture ratio. In addition, such an increase in a storage capacitor value can remove a flicker and a residual image to improve picture quality, thereby realizing a high picture quality.

[0071] It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.